TE (Elect), Sem - III, A.Y. K.T. 26/6/15 Lib 26/06/15
Power Electronics

Bharatiya Vidya Bhavan's

SARDAR PATEL COLLEGE OF ENGINEERING

(An Autonomous Institution Affiliated to University of Mumbai)

Total Marks: 100 | KT EXAM: JUNE 2015 | Duration: 3 Hours

CLASS/SEM: TE/VI SEM (Elect), | SUBJECT: POWER ELECTRONICS

- Question no.1 is compulsory
- Attempt any Four question out of Six questions
- Answers to all sub questions should be grouped together
- Assume suitable data if necessary and justify the same

Master.

Q1) A) Explain qualitatively (no mathematical approach), what will happen if a free-wheeling diode (cathode of the diode shorted with the cathode of the thyristor) is connected across the load in rectifier circuit. 5

B) Draw output current and voltage waveform for the following load when it is fed by **controlled half wave rectifier.** 6
- RL load
- Pure L load

C) Explain the operation of single phase half bridge inverter with RL Load 6

D) Explain effect of source impedance on 3 phase full controlled converter. 3

Q2) A) Write short note on SCR using following points 8
- V-I characteristics
- Latching and holding current of SCR

B) Draw output voltage waveform of 3 phase 6 pulse controlled converter when, (USE GRAPH PAPER) 12
1. $\alpha = 0^0$
2. $\alpha = 90^0$

Q3) A) Explain current source inverter. What are its advantages and disadvantages w.r.t. voltage source inverter. 10

B) Write short note on single phase dual converter with the help of circulating current mode. 10

Q4) A) Explain sinusoidal sine-triangular PWM. 10

B) Explain principle of phase control. And explain single phase full wave controller with RL load. 10

Q5) A) What are the performance parameters of inverters? 8

B) Explain six step operation of inverter. Explain it with pole voltage and line 12

TE(Elect), Sem-VI, A.T.K.T, 25/6/18.
Power Electronics.

voltage waveforms. (USE GRAPH PAPER)

Q6)	A)	What are the performance parameters of a rectifier? Explain the significance of each parameter.	10
	B)	The Buck regulator has an input voltage of V_s=12V .The required average output voltage is 5V at R=500Ω and peak to peak output ripple voltage is 20mV. The switching frequency is 25 KH_z. If peak to peak ripple current of inductor is limited to 0.8A .Determine duty cycle and critical values of L and C.	10
Q7)	A)	A single phase full converter is supplied from 230V, 50H_z source. The load consist of R=10Ω and a large inductance so as to render the load current constant. For a firing angle delay of 30°, Determine average output voltage ,average output current and power fact	12
	B)	The single phase half bridge inverter has a resistive load of R=2.4Ω and the DC input voltage is V_s=48V. Determine (a) r.m.s. output voltage (b) the output r.m.s. power P_0	8

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15/06/15

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SARDAR PATEL COLLEGE OF ENGINEERING

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Re-Exam

TE (Elect), Sem. VI, Re-exam, 15/6/15

Power System operation Control.

TOTAL MARKS : **100** DURATION : **3 Hours**

CLASS/SEM : **T.E.** Electrical/Sem-**VI** SUBJECT :**PSOC**

Question *one* is compulsory. Attempt any *four* questions from remaining *six* questions

Master

5*4

Q1 a) Explain loadibility curves for transmission lines.

b) Name different operating states of power system and also control strategy for respective states.

c) Derive co-ordinate equation considering the transmission losses.

e) Rotor angle stability and voltage stability are interdependent .Justify

Q2 a) Draw and explain voltage –power characteristic for radial line with fixed sending end voltage. 10

b) Explain merits and demerits of series compensated system. 10

Q3 a) Derive the complete block diagram representation for load frequency control of a single area system. 15

b) Explain how steady state error can be reduced for the above case. 5

Q4 a) Using a neat schematic diagram, derive block diagram for alternator voltage regulator. 10

b) Explain with the help of neat diagrams the reactive capability limits of synchronous machines. 10

Q5 a) Explain with the help of neat diagrams working of TCSC and its characteristic. 10

b) What were the reasons for deregulating the Indian power sector? 12

Q6 a) Incremental cost in rupees per MWh for a plant consisting of two units are:

$dC_1/dP_1=0.2P_1+40$

$dC_2/dP_2=0.4P_2+30$ and the generator limits are as follows:

$30MW \leq P_1 \leq 175MW$

$20MW \leq P_2 \leq 125MW$

Assume that both units are operating at all times. How will the load be shared between the two units as the system load varies over the full range of the load values? What are the corresponding values of the plant incremental costs? 8

b) For the Q6(a),find the saving in fuel cost in rupees per hour for the optimal Scheduling of a total load of 175MW as compared to equal distribution of the same load between the two units. 2*10

Q7 Write short note on any two:-

i)Static Var Systems

ii)Static synchronous condensers

iii)Phase shifting transformer

page 1

TE (Elect), Sem-VI, 27/4/2015.
Power System Operation & Control.

chb 27/04/15

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TOTAL MARKS : **100** DURATION : **3 Hours**

CLASS/SEM : **T.E.** (Electrical) / Sem-VI SUBJECT :**PSOC**

Attempt any ***FIVE*** questions out of ***SEVEN*** questions.

- First question is compulsory.
- Figures to the right indicate full marks.
- . Answers to all sub questions should be grouped together

Master

Q1 a) Compare performance of HVDC Link with TCSC compensated line. 4x5

b) Find the reactive power requirement of the line with sources at both the ends?

c) How series capacitors can be protected against over voltages.

d) Explain with the help of neat diagram working of TCSR.

Q2 a) Derive the complete block diagram representation for load frequency control of a two area system. 12

b) Explain SSR and its effects in a series compensated system. 8

Q3 a) How TCR can be used to maintain voltage profile of the line and explain its V-I characteristic .Mention a method to reduce harmonics in TCR compensated system. 10

b) Derive a general expression for transmission loss of a system having 'k' plants interconnected. 10

Q4 a) Explain with the help of neat block diagram overload prevention in line connected in parallel to a TCSC compensated lines .Also elaborate the use of give up function and auxiliary controller. 14

b) Derive the coordination equation for the economic load scheduling of power plants, neglecting transmission losses. 6

Q5 a) Incremental fuel cost in rupees per MWh for a plant consisting of two units are: 12

$$\frac{dC_1}{dP_{G1}} = 0.20P_{G1} + 40.0 \qquad \frac{dC_2}{dP_{G2}} = 0.25P_{G2} + 30.0$$

Assume that both units are operating at all times, and total load varies from 40MW to 250 MW, and the maximum and minimum loads on each unit are to be125and20MW,respectively. How will the load be shared between the two units as the system load varies over the full range? What are the corresponding values of the plant incremental costs?

b) Give the structure of a deregulated power sector and also explain the entities involve in it. 8

TE(E|EC4) Sem-VI, 27/4/15
Power System operation & Control.

Q6	a)	Explain with the help of a neat diagram working of TSSC and also explain its V-I characteristic.	10
	b)	Describe the use of shunt reactors and shunt capacitor in EHV over head lines. Also give advantages and disadvantages of this type of compensation	10
Q7	a)	Explain with the help of neat diagram different excitation systems used for synchronous generators.	10
	b)	Write a short note on Phase shifting transformer and also explain how it can be used to control power flowing through a line.	10

Lib
16/06/15

TE(Elect), Sem-VI, Re-exam, 16/6/15

Control System - II

BHARATIYA VIDYA BHAVAN'S

SARDAR PATEL COLLEGE OF ENGINEERING

Munshi Nagar,Andheri(West),Mumbai 400 058

[An Autonomous Institution Affiliated to University of Mumbai]

RE-EXAMINATION

SEM/CLASS: VI/ T.E. Electrical

SUBJECT: Control System - II

TOTAL MARKS: 100

DURATION : 3 HOUR

DATE : 16/06/2015

Note:

1. Answer any five questions out of seven.
2. Figures to the right indicate full marks.
3. Assume suitable data if necessary and justify the same.
4. Answers to all sub-questions should be grouped together.

Master

Q. 1 a) The closed loop frequency response |M(jw)| versus frequency of a second order prototype system is shown in **Fig. 1.**

Find out the peak time, percentage overshoot, settling time and steady- state error for unit step .

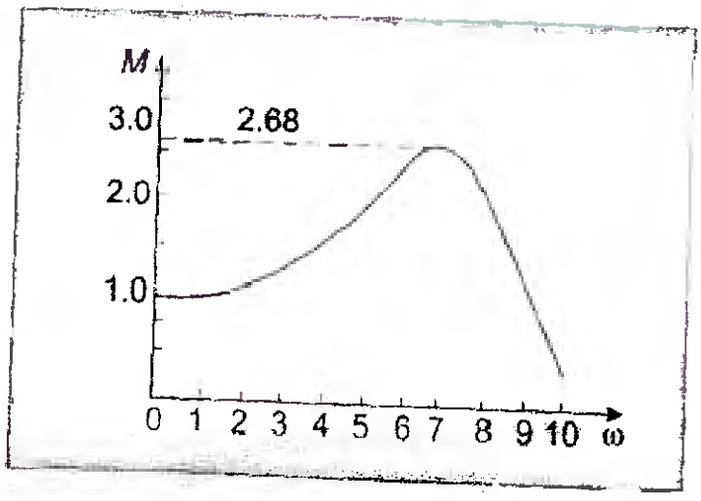


Fig. 1

(10)

TE(Elect), Sem-VI, Re-exam, 16/6/15
Control System-II

Q. 1 b) Describe Eigen Values and Eigen Vector in brief. (06)

Q. 1 c) Given $G(s) = \dfrac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$. Show that $|G(j\omega_n)| = \dfrac{1}{2\xi}$ (04)

Q. 2 a) Explain the importance of observer in state space design. (04)

Define Controllability and Observability. (04)

Derive $K_z = K_x P^{-1}$ where K_z is feedback gain vector of the system which is not represented in phase variable form, K_x is feedback gain vector of the system which is represented in phase variable form and P is a transformation matrix between these two state space representations of same physical system. **(06)**

Q. 2 b) Sketch the polar Nyquist plot for the open loop transfer function given below.

$$G(s) = \frac{10}{s(s+1)(1+0.5s)}$$ **(06)**

Q. 3 a) Derive the relation for solution of state space equation for linear time invariant system. **(05)**

Q. 3 b) List out the frequency domain analysis specifications. Define Principal of Argument and state Nyquist stability criterion for minimum phase system. **(05)**

Q. 3 b) For a system represented by the state equation

$$\dot{x} = Ax .$$

The response of $x(t) = \begin{bmatrix} e^{-2t} \\ -2e^{-2t} \end{bmatrix}$ *when* $x(0) = \begin{bmatrix} 1 \\ -2 \end{bmatrix}$

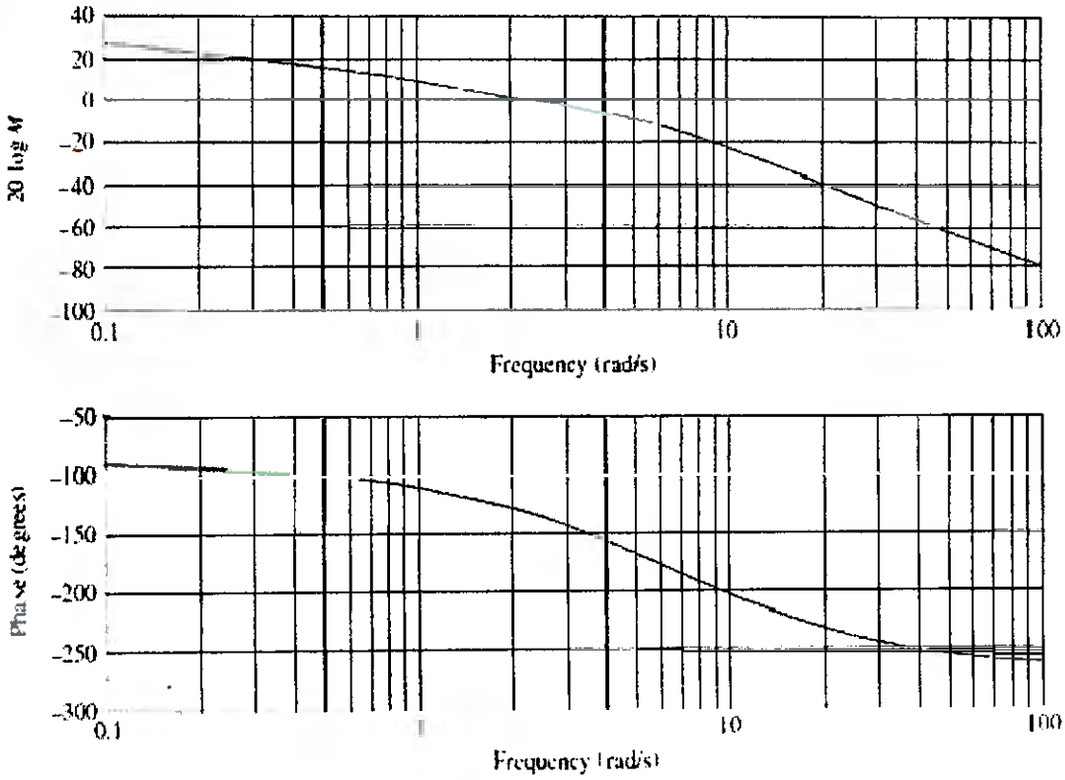
and $x(t) = \begin{bmatrix} e^{-t} \\ -e^{-t} \end{bmatrix}$ *when* $x(0) = \begin{bmatrix} 1 \\ -1 \end{bmatrix}$

Determine the system matrix **A** and the state transition matrix. **(10)**

TE (E&C), Sem - VI, Re-Exam, 16/6/15
Control System - II

Q. 4 a) Derive the expression for constant **M-Circle**. **(07)**

Q. 4 b) The Bode plots for a plant, G(s), used in a unity feedback system are shown in



Do the following:

a. Find the gain margin, phase margin, zero dB frequency, 180 degree frequency, and the closed-loop bandwidth. **(05)**

b. Use your results in Part a to estimate the damping ratio, percent overshoot, settling time, and peak time. **(08)**

Q. 5) Consider the unity feedback system with G(s) as forward path transfer function with

$$G(s) = \frac{K}{s(s+5)(s+20)}$$

The uncompensated system has about 55% overshoot and a peak time of 0.5 second when Kv= 10. Use frequency response methods to design a lead compensator to reduce the percent overshoot to 10%, while keeping the peak time and steady state error about the same or less. **(20)**

Page (3)

TE (Elect), Sem-VI, Re-Exam, 16/6/15
Control System-II

Q. 6) Use frequency response methods to design a lag-lead compensator for a unity feedback system where forward path transfer function is given as

$$G(s) = \frac{K(s+7)}{s(s+5)(s+115)}$$

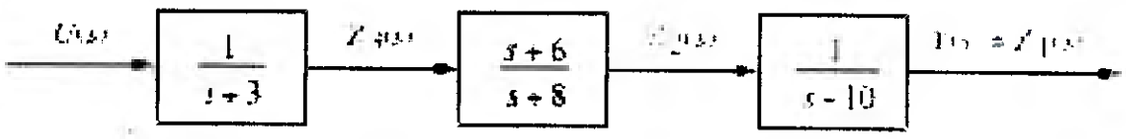
and the following specifications are to be met:
Percent overshoot = 15%, settling time= 0.1 second, and Kv= 1000.

(20)

Q. 7) Consider the following transfer function:

$$G(s) = \frac{(s+6)}{(s+3)(s+8)(s+10)}$$

If the system is represented in cascade form as shown in figure below



Consider $Z_1(s) = Y(s), Z_2(s)$ *and* $Z_3(s)$ as state variables for designing the controller. Design a controller to yield a closed loop response of **10% overshoot** with a **settling time of 1 second.** Design the controller by first transforming the plant to phase variable.

(20)

2.b
29-4-15.

TE(Elect), Sem-VI
Control System-II

BHARATIYA VIDYA BHAVAN'S

SARDAR PATEL COLLEGE OF ENGINEERING

Munshi Nagar,Andheri(West),Mumbai 400 058

[An Autonomous Institution Affiliated to University of Mumbai]

END SEMESTER EXAMINATION

SEM/CLASS: VI/T.E./Electrical — TOTAL MARKS: 100

SUBJECT: Control System - II — DURATION : 3 HOUR

DATE : 29/04/2015

Note:

1. Answer any five questions out of seven.
2. Figures to the right indicate full marks.
3. Assume suitable data if necessary and justify the same.
4. Answers to all sub-questions should be grouped together.

Master

Q. 1 a) The closed loop frequency response |M(jw)| versus frequency of a second order prototype system is shown in **Fig. 1.**

Find out the peak time, percentage overshoot, settling time and steady- state error for unit step .

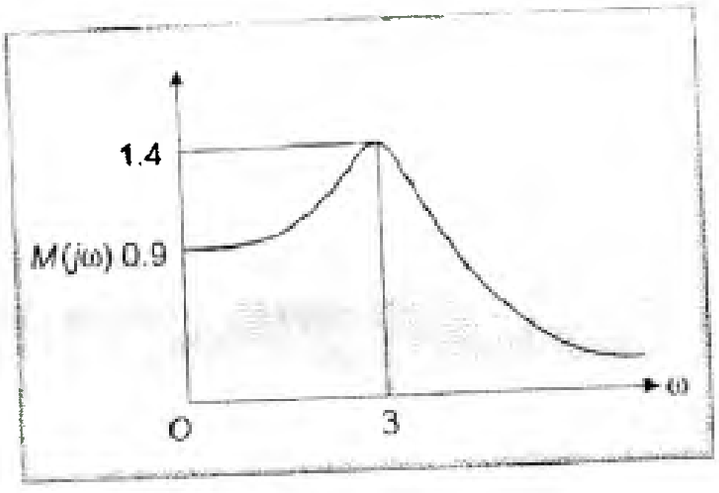


Fig. 1

(10)

TE (Elect) Sem-VI, 29/4/15
Control System-II

Q. 1 b) Describe Elgen Values and Eigen Vector in brief. **(04)**

Q. 1 c) Derive the expression for modal matrix for diagonalizing any square matrix with distinct elgen values. **(06)**

Q. 2 a) Explain the importance of observer in state space design. Discuss in details the steps for designing the observer gain vector if plant is not represented in observer canonical form. **(10)**

Q. 2 b) Sketch the polar Nyquist plot for the open loop transfer function given below and comment on the closed loop stability of unity feedback system.

$$G(s) = \frac{10}{s(s+1)(1+0.5s)}$$ **(10)**

Q. 3 a) A control system is described by the differential equation

$$\frac{d^3y(t)}{dt^3} = u(t)$$

where y(t) is the observed output and u(t) is the input.

1. Describe the system in state space form
2. Is the system controllable?
3. Is the system Observable?

(10)

Q. 3 b) Explain with mathematical justification why **"s"** is replaced with **"jw"** in frequency domain analysis of the control system. **(10)**

Q. 4 a) Derive the expression for constant M-Circle. **(07)**

Q. 4 b) Consider the plant **(13)**

$$G(s) = \frac{1}{s(s+3)(s+7)}$$

whose state variables are not available. Design an observer for the observer canonical variables to yield a transient response described by **damping ration of 0.4** and **natural frequency of**

TE(E/ele), Sem-VI, 29/4/15
Control System - II

oscillations is 75. Place the third pole 10 times farther from the imaginary axis than the dominant poles.

Q. 5) The transfer function from applied force to arm displacement for the arm of a hard disk drive has been identified as

$$G(s) = \frac{X(s)}{F(s)} = \frac{3.333 \times 10^4}{s^2}$$

The position of the arm will be controlled using the unity feedback loop with G(s) as forward path transfer function.

Design a **lead compensator** to achieve closed-loop stability with a transient response of **16%** overshoot and a settling time of **2 msec** for a step input.

(20)

Q. 6) An electric ventricular assist device (EVAD) that helps pump blood concurrently to a effective natural heart in sick patients can be shown to have a transfer function.

$$G(s) = \frac{P_{ao}(s)}{E_m(s)} = \frac{1361}{s^2 + 69s + 70.85}$$

The input, Em(s), is the motor's armature voltage, and the output is Pao(s), the aortic blood pressure (Tasch, 1990). The EVAD will be controlled in the closed-loop configuration with unity feedback loop with G(s) as forward path transfer function.

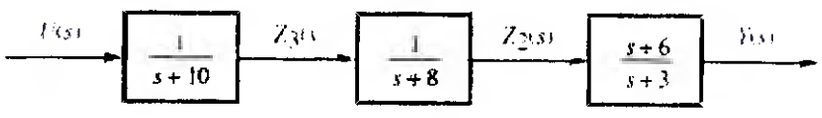
Design a phase lag compensator to achieve a **tenfold improvement** in the steady-state error to step inputs without appreciably affecting the transient response of the uncompensated system

(20)

Q. 7) Consider the following transfer function: **(20)**

$$G(s) = \frac{(s+6)}{(s+3)(s+8)(s+10)}$$

If the system is represented in cascade form as shown in figure below



Consider $Z_1(s) = Y(s), Z_2(s)$ *and* $Z_3(s)$ as state variables for designing the controller. Design a controller to yield a closed loop response of **10% overshoot** with a **settling time of 1 second**. Design the controller by first transforming the plant to phase variable.

TE (Elect), Sem-VI, Re-Exam, 17/06/15
Microcontroller & Applications.

Lib 17/06/15

Bharatiya Vidya Bhavan's

SARDAR PATEL COLLEGE OF ENGINEERING

(An Autonomous Institution Affiliated to University of Mumbai)

Total Marks: 100 REEXAM: JUNE 2015 Duration: 3 Hours

CLASS/SEM: TE/VI/SEM (Elect) SUBJECT: MICROCONTROLLER & APPLICATIONS

- Question no.1 is compulsory
- Attempt any Four question out of Six questions
- Answers to all sub questions should be grouped together
- Assume suitable data if necessary and justify the same

Master

Q1.a) Show the contents of PSW register after the execution of following instructions. 5

MOV A, #0BFH

Add A, #1BH

b) How is the stack used in the case of a CALL (LCALL or ACALL) instruction? 5

c) Show code (program) for a nested loop to perform an action for **500** times. 5

d) Write a program in assembly level to create square wave of 66% duty cycle on 8051 microcontroller' bit 3 of port 1. 5

Q2)a) Write short note on port 1 of 8051 microcontroller. 10

b) A switch is connected to in P1.0 and LED to P2.7. Write a program in assembly level to get the status of the switch and send it to LED. 8

c) Name bit 4 addressable registers. 2

Q3) Write short note 20

1. TMOD
2. Control word register of 8255
3. PSW

TE(Elect) Sem-VII, 17/06/15, Re-exam,
Microcontroller & Application.

Q4a)	Explain interfacing of external memory to 8051.	10
b)	Explain interfacing of stepper motor with 8051 microcontroller.	10
Q5)a)	Explain addressing modes of 8051 microcontroller.	12
b)	Write C program to get the status of bit P1.0, save it, and send it to P2.7continuously.	8
Q6a)	Compare Microcontroller with Microprocessor.	10
b)	Explain interfacing of DAC with 8051.	10
Q7)	Write short note on 1. Keyboard interfacing with 8051 2. 8051 architecture	20

TE(Elect), Sem - VI, 2015
Microcontroller & Application

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02-05-15.

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SARDAR PATEL COLLEGE OF ENGINEERING

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Total Marks: 100 Duration: 3 Hours

CLASS/SEM TE/VI SEM (Elect) SUBJECT: MICROCONTROLLER & APPLICATIONS

- Attempt any FIVE question out of SEVEN questions
- Answers to all sub questions should be grouped together
- Figures to the right indicate full marks
- Write program in embedded C wherever mentioned in question

Master

Q1. a) With the help of neat sketch design stepper motor interfacing to port A of 8255 IC. Write a program to rotate the motor in clockwise direction. 10

b) Design interfacing circuit of 8051 with 8255 such that port A is selected for address COH, port B is selected for address C2H,port C for address C4H and control register for address C6H 10

Q2) a) Write a program to create square wave of 66% duty cycle on 8051 microcontroller' bit 3 of port 1. 10

b) Interface DAC 08 using port B of 8255 and write a program to generate ramp wave. 10

Q3) a) Explain following jump instructions 8

1) JNC 2) JZ 3) LJMP 4) SJMP

b) Write short note on different types of addressing modes in 8051with examples. 12

Q4a) Write short note on port 3. 10

b) Write an 8051 C program to toggle all the bits of P0 & P2 continuously with a250 ms delay, use inverting operator. 10

TE(Elect), Sem VI 215/15

Microcontroller & Application

Q5) a)	Generate a square wave with an on time of 3 ms & the off time of 10 ms on all pins of port 0. XTAL frequency can be taken as 22MHz.	14
b)	Write an 8051 c program to turn bit P1.5 on and off 50000 times.	6
Q6)a)	Explain in detail following SFR (special function registers) 1. PSW 2. TMOD	10
b)	Explain matrix keyboard interfacing	10
	OR	
	Compare microcontroller with general purpose microprocessor,	
Q7)a)	Write a program to add two 32 bits numbers, 01453BC0 H & 56C705FE H, which are stored in RAM location 40H and above. And store its result in RAM address 60H and above.	13
b)	Assume register A has packed BCD :29H .Write a program to convert packed BCD to two ASCII numbers & place them in registers R2 &R6 .	7

Lib 18/06/15

TE(Elect), Sem- VI, Re-exam, 18/6/15

Communication Engineering

BHARATIYA VIDYA BHAVAN'S

SARDAR PATEL COLLEGE OF ENGINEERING

[An Autonomous Institution Affiliated to University of Mumbai]

Reexamination

SEM/CLASS: VI/TE ELECTRICAL.
SUBJECT: **Communication Engineering.**

TOTAL MARKS: 100.
DURATION: **3Hours.**
DATE : **June, 2015.**

Note: Solve any Five Questions.

Master

Q1: a>What is channel capacity? Derive an expression for channel capacity of noisy Channel. (10)

b>Seven messages are to be transmitted, one message at a time. Develop binary and quaternary Huffman code for seven messages with probabilities 0.2, 0.35, 0.13, 0.12, 0.11, 0.05, 0.04. Calculate code efficiency in each case. (10)

Q2: a>Define amplitude modulation and modulation index. Derive the relation between the output power of an AM transmitter and the depth of modulation. (10)

b>With a neat block diagram explain Independent Side Band (ISB) system. (10)

Q3: a>Explain FET reactance modulator as a capacitive reactance and describe how should it be used in practice. (10)

b>Draw the block diagram and explain Armstrong modulating system. (10)

Q4: a>Draw block diagrams and compare tuned radio frequency and superheterodyne radio receivers. (10)

b> Calculate carrier and modulating frequencies, modulation index and maximum deviation of FM wave represented by the following voltage equation:

$$V = 10sin(10 \times 10^8 t + 15sin1250t) \quad \textbf{(05)}$$

c>Explain frequency division multiplexing (FDM). (05)

Q5: a>Define and describe pulse position modulation. Explain with waveforms how it is derived from pulse width modulation. (10)

b>Explain the working of delta modulation system and discuss the errors produced by the same. (10)

Q6: a> With block diagram explain BPSK modulator-demodulator. (10)

b> Compare the system BPSK, ASK, BFSK, DPSK based on output of transmitter, bandwidth, distance in signal space between two symbols. (10)

Q7: a> Generate systematic codeword from (7,4) code word system with $g(x) = 1 + X^2 + X^3$ and message vector m=1011. (10)

b With an example explain convolution code. (10)

TE(Elect), Sem - VI, 5/5/15
Communication Engineering

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05/05/2015

BHARATIYA VIDYA BHAVAN'S

SARDAR PATEL COLLEGE OF ENGINEERING

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END SEMESTER EXAMINATION

SEM/CLASS: **VI/TE ELECTRICAL.** TOTAL MARKS: **100.**

DURATION: **3Hours.** DATE:,**05/05/2015.**

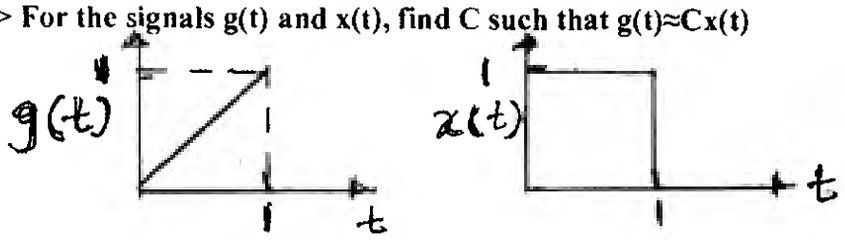
SUBJECT: **Communication Engineering**

Master

Note: Question No. 1 is compulsory. Solve any Four Questions out of remaining Six Questions.

Q1: a>The bit pattern 01110010 is modulated using digital modulation techniques. The carrier frequency is twice the bit frequency. Draw the output of BPSK, DPSK, QPSK systems. (06)

b> For the signals g(t) and x(t), find C such that g(t)≈Cx(t) (04)



c> How does companding reduce quantization error? (02)

d> Explain double spotting in radio receivers. (02)

e> An AM transmitter has an unmodulated carrier signal power Pc=100W. Three modulating signals of modulation indices 0.25, 0.4 and 0.5 are modulated using this carrier. What is the total power of modulated signal? (02)

f> The signal $x(t) = 10\cos(2000\pi t)\cos(6000\pi t)$ is sampled based on low pass uniform sampling theorem. What is the minimum sampling rate required? (02)

g> What is the difference between source coding and channel coding? (02)

Q2: a> With a neat block diagram explain the "third" method of SSB generation. (06)

b> Draw the block diagram of Super heterodyne radio receiver and explain its working. Write frequency component present at the output of each block if the audio frequency is 1.5 KHz and carrier frequency is 535 KHz. (06)

c> The mutual conductance of FET varies linearly with gate voltage between 0 to 10 mS. The FET is used as capacitive reactance modulator with $Xc_{gd}=10\ R_{gs}$. and is placed across an oscillator which is tuned to 40MHZ by a 50μF fixed capacitor. What will be the total frequency variation when transconduction of the FET is varied from 0 to maximum by modulating voltage. (08)

Q3: a> What is pulse width modulation? How is it generated and demodulated? (10)

b> With an example and waveforms explain pulse code generation and demodulation. (10)

Q4: a> What is entropy? Derive the expression for entropy. Show that entropy is maximum when all the messages are equiprobable. (06)

TE (Elect), Sem - VI, 5/5/15

Communication Engineering

b> A high resolution black and white picture consists of about $4x10^6$ picture elements and 32 different brightness pictures required at the rate of 64/sec. All picture elements are assumed to be independent and all levels have equal likelihood of occurrence. Calculate average rate of information conveyed by this TV picture source. (06)

c> Two messages m1 and m2 with probabilities 0.7 and 0.3 are coded with Huffman coding. If the source is of N messages. Calculate code efficiency when (08)
(i) N=1 (ii) N=2

Q5: a> Consider a sinusoidal signal $x(t) = A \cos w_o t$ is applied to a delta modulator with a step size of δ. Show that the slope overload distortion will occur if $A > \frac{\delta}{w_o T_s}$, where T_s is sampling rate. (05)

b> Compare FDM and TDM methods of multiplexing. (05)

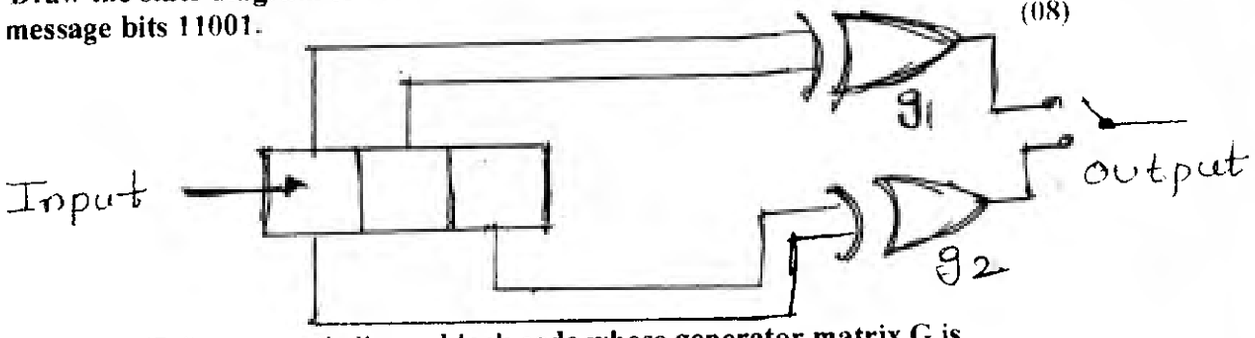
c> Why and how delta modulation is replaced by adaptive delta modulation? (10)

Q6: a> Explain offset QPSK (OQPSK) transmitter and receiver with appropriate waveforms. Differentiate OQPSK with BPSK based on signal space representation and bandwidth. (12)

b> Compare receivers of BPSK and DPSK. (04)

c> With a neat block diagram explain FSK receiver. (04)

Q7: a> Draw the state diagram for convolution encoder shown below. Write the code for message bits 11001. (08)



b> Consider (7,4) systematic linear block code whose generator matrix G is

$$G = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

(i) Find all code words of code. (04)
(ii) Find H parity check matrix. (02)
(iii) Compute syndrome for the received vector 1101101. (02)
(iv) Is this a valid codeword? Why? (02)
(v) What is the error detection and correction capability of code? (02)

TE (Elect), Sem-VI, Re-exam, 21/6/15. Lib 21/6/15
Digital Signal Processing.

Bharatiya Vidya Bhavan's

Sardar Patel College of Engineering

(Govt. Aided Autonomous Institute Affiliated to University of Mumbai)

Re-Examination June 2015 Master

Subject: Digital Signal Processing **Class:** T.E. (Electrical, Sem: VI)

Date: 19th June 2015 **Total Marks:** 100

Note: Solve any FIVE questions of the following. Group the answers to all sub-questions together.

---

1. Design an FIR lowpass filter using Kaiser Window Function to satisfy following specifications: $A_p \le 0.1dB$ at 20 *rad/sec* and $A_s \ge 44\,dB$ for 30 *rad/sec*. Assume sampling frequency of 100 *rad/sec*. **(20)**

2. Design an analog lowpass filter using Chebyshev Type – I and Chebyshev Type – II approximation to meet following specifications: $A_p \le 1$ *dB* for $\Omega_p \le 4$ *rad/s* and $A_s \ge 20$ *dB* for $\Omega_s \ge 8$ *rad/s*. **(20)**

3. *a.* Using Hanning Window Function, design a sixth order linear phase FIR lowpass filter having cutoff frequency of $\frac{\pi}{4}$ rad. **(10)**

   b. Find the output $y(n)$ of a filter whose impulse response is $h(n)=\{1,1,1\}$ and input signal $x(n)=\{3,-1,0,1,3,2,0,1,2,1\}$ using overlap-save method and overlap-add method. **(10)**

4. *a.* Given that $x_1(n)=\{1,2,2,1\}$ and $x_2(n)=\{1,2,3,1\}$. Find $x_3(n)$ such that $X_3(k)=X_1(k).X_2(k)$. **(10)**

   b. Determine 8-point DFT of the sequence $x(n)=\{1,2,4,,8,16,32,64,128\}$ using radix-2 DIT FFT algorithm. **(10)**

TE CE(Elect), sem-VI, Re-exam, 2016/15.
Digital Signal processing

5. *a.* For the system described by the difference equation, **(10)**

$$y(n)-\frac{1}{2}y(n-1)+\frac{1}{4}y(n-2)=x(n),$$

Determine, *i.* transfer function and

ii. response of the system to the input $x(n)=\left(\frac{1}{3}\right)^n u(n)$.

b. Determine and sketch the magnitude and phase response of the sequence given below: **(10)**
$y(n)=x(n)+0.9x(n-2)-0.4y(n-2)$.
[**Note:** Plot the magnitude and phase response on a graph paper only.]

6. *a.* An analog circuit has following normalized, s-plane transfer function: **(10)**

$$H(s)=\frac{5s+1}{s^2+0.4s+1}$$

Determine the transfer function of an equivalent digital circuit using BLT with resonant frequency of 10 Hz and sampling frequency of 60 Hz

b. Design an equivalent digital filter from an analog filter $H(s)=\frac{1}{s^2+\sqrt{2}s+1}$ using *impulse invariance method.* Assume T = 1 sec. **(10)**

7. *a.* (*i*) State and prove symmetry properties of DFT for a real valued sequence. **(10)**
(*ii*) The first 8 samples of a 14-point DFT $X(k)$ of a real valued sequence $x(n)$ are:

$X(0)=12,\quad X(1)=-1+j3,\quad X(2)=3+j4,\quad X(3)=1-j5,$

$X(4)=-2+j2,\quad X(5)=6+j3,\quad X(6)=-2-j3,\quad X(7)=10,$

Determine remaining samples of DFT $X(k)$

b. Determine linear convolution of the following signals using convolution property of DTFT. **(10)**
$x_1(n)=nu(n)$ and $x_2(n)=(2)^n u(n-1)$.

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TE(Elect), sem - VI, 8/5/15
Digital Signal Processing

HB
08/05/15

Bharatiya Vidya Bhavan's

Sardar Patel College of Engineering

(Govt. Aided Autonomous Institute Affiliated to University of Mumbai)

End Semester Examination May 2015 MASTER FILE

Subject: Digital Signal Processing
Class: T.E. (Electrical, Sem: VI)
Date: 7th May 2015
Total Marks: 100

Note: Solve any of following questions **(maximum five)** such that the total attempt is of 100 marks.

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1. Design an FIR lowpass filter using Kaiser Window Function to satisfy following specifications: $A_p \le 0.1\,dB$ at 20 *rad/sec* and $A_s \ge 44\,dB$ for 30 *rad/sec*. Assume sampling frequency of 100 *rad/sec*. **(20)**

2. *a* Using frequency sampling method determine the coefficients and draw realization diagram of a linear-phase FIR filter of length 15 which has a symmetric unit sample response and a frequency response that satisfies the condition, **(10)**

$$H\left(\frac{2\pi k}{15}\right) = \begin{cases} 1, & k = 0,1,2,3 \\ 0.4, & k = 4 \\ 0, & k = 5,6,7 \end{cases}$$

b Design a linear phase FIR highpass filter using Hanning window function, for the specifications given below: **(10)**
Stopband edge = 2 kHz, Stopband attenuation ≥ 40 dB, Passband edge = 9.5 kHz,
Passband attenuation < 1 dB, Sampling frequency = 25 kHz.

3. *a* Design a Butterworth digital IIR highpass filter using bilinear transformation by taking T = 0.5 sec, to satisfy following specifications: **(10)**

$$0.707 \le \left|H\left(e^{j\omega}\right)\right| \le 1.0 \qquad ;0.65\pi \le \omega \le \pi$$

$$\left|H\left(e^{j\omega}\right)\right| \le 0.2 \qquad ;0 \le \omega \le 0.45\pi$$

b. Design a Chebyshev digital IIR lowpass filter using bilinear transformation by taking T = 1 sec, to satisfy following specifications: **(10)**

$$0.8 \le \left|H\left(e^{j\omega}\right)\right| \le 1.0 \qquad ;0 \le \omega \le 0.2\pi$$

$$\left|H\left(e^{j\omega}\right)\right| \le 0.2 \qquad ;0.32\pi \le \omega \le \pi$$

TE (E&TC) Sem - VI 8/5/15

Digital Signal processing

4. *a.* Determine the response of an LTI system by radix-2 DIT FFT algorithm to the input $x(n)=\{-1,2,2,2,-1\}$, if its impulse response is $h(n)=\{-1,1,-1,1\}$. **(30)**

b. Determine the transfer function and sketch poles and zeros of an LTI system described by the equation, $y(n)=x(n)+0.8x(n-1)+0.8x(n-2)-0.49y(n-2)$. Comment on the stability of this system. **(10)**

5. *a.* Find circular convolution of following two sequences using DFT/IDFT method. Use DIT-FFT algorithm to find DFT and DIF-FFT algorithm to find IDFT. $x_1(n)=\{0,1,0,1\}$ and $x_2(n)=\{1,2,1,2\}$. **(10)**

b Determine and sketch the magnitude and phase response of the sequence given below: **(10)**
$y(n)=x(n)+0.9x(n-2)-0.4y(n-2)$.
[**Note:** Plot the magnitude and phase response on a graph paper only.]

6. *a.* Convert the analog filter with system function, $H(s)=\dfrac{1}{(s+0.5)(s^2+0.5s+2)}$ into a digital IIR filter using impulse invariance method, with $T_s=1\text{sec}$. **(10)**

b A simple LRC notch filter has following normalized, s-plane transfer function: **(10)**

$$H(s)=\frac{s^2+1}{s^2+s+1}$$

Determine the transfer function of an equivalent digital filter using BLT. Assume a notch frequency of 60 Hz and sampling frequency of 960 Hz

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TE (Elect), Sem - VI, 9/5/15
Protection & Switchgear Engineering

Lib 09/05/15 (Old)

BHARARATIYA VIDYA BHAVAN'S

SARDAR PATEL COLLEGE OF ENGINEERING

Munshi Nagar Andheri (West), Mumbai 400 058

(An Autonomous Institution Affiliated to University of Mumbai)

End Sem Examination

CLASS/SEM: **TE (Electrical)/ VI/OLD**
Subject: **Protection and Switchgear Engineering**

Total Marks: **100**
Duration : **3 hour**

Master

- Attempt any 5 questions
- Best of luck!

1.	a.	Explain any 3 electromagnetic type relay.	[12]
	b.	What is primary and back up protection?	[8]
2.	a.	Explain phenomenon of arcing ground?	[5]
	b.	What is MHO relay?	[5]
	c.	Write a note on directional relay?	[10]
3.	a.	Which are the types of over current relay according to the time-current characteristics? Explain.	[12]
	b.	Write the principle of Buchholz relay.	[8]
4.	a.	What is single phasing? How the motor can be protected from single phasing?	[10]
	b.	Explain biased differential relay?	[10]
5.	Write a note on		
	a.	Transient restriking voltage	[5]
	b.	Current chopping	[5]
	c.	Making and breaking capacity of a circuit breaker	[5]
	d.	Slepain's theory	[5]

TE (Elect), Sem - VI, 9/5/15 (old)
Protection & Switchgear Engineering

6	a.	Explain the construction and working of air break circuit breaker?	[10]
	b.	Write the principle of arc quenching in oil circuit breaker?	[10]
7		Explain lightning phenomenon and different types of lightning arresters	[20]